

September 1988

Software Serial Port Implemented with the PCA

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For microcontroller applications which require more than one serial port, the 83C51FA Programmable Counter Array (PCA) can implement additional half-duplex serial ports. If the on-chip UART is being used as an inter-processor link, the PCA can be used to interface the 83C51FA to additional asynchronous lines.

This application uses several different Compare/Capture modes available on the PCA to receive or transmit bytes of data. It is assumed the reader is familiar the PCA and ASM51. For more information on the PCA refer to the "Hardware Description of the 83C51FA" chapter in the Embedded Controller Handbook (Order No. 210918).

Introduction

The figure below shows the format of a standard 10-bit asynchronous frame: 1 start bit (0), 8 data bits, and 1 stop bit (1). The start bit is used to synchronize the receiver to the transmitter; at the leading edge of the start bit the receiver must set up its timing logic to sample the incoming line in the center of each bit. Following the start bit are eight data bits which are transmitted least significant bit first. The stop bit is set to the opposite state of the start bit to guarantee that the leading edge of the start bit will cause a transition on the line. It also provides a dead time on the line so that the receiver can maintain its synchronization.

Two of the Compare/Capture modes on the PCA are used in receiving and transmitting data bits. When receiving, the Negative-Edge Capture mode allows the PCA to detect the start bit. Then using the Software Timer mode, interrupts are generated to sample the incoming data bits. This same mode is used to clock out bits when transmitting.

This Application Note contains four sections of code:

- (1) List of variables
- (2) Initialization routine

- (3) Receive routine
- (4) Transmit routine.

A complete listing of the routines and the test loop which was used to verify their operation is found in the Appendix. A total of three half-duplex channels were run at 2400 Baud in the test program. The listings shown here are simplified to one channel (Channel 0).

Variables

Listing 1 shows the variables used in both the receive and transmit routines. Flags are defined to signify the status of the reception or transmission of a byte (e.g. RCV_START_BIT, TXM_START_BIT). RCV_BUF and TXM_BUF simulate the on-chip serial port SBUF as two separate buffer registers. The temporary registers, RCV_REG and TXM_REG, are used to save bits as they are received or transmitted. Finally, two counter registers keep track of how many bits have been received or transmitted.

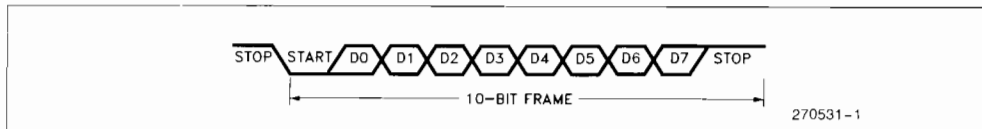
Variables are also needed to define one-half and one-full bit times in units of PCA timer ticks. (One bit time = $1 / \text{baud rate}$.) With the PCA timer incremented every machine cycle, the equation to calculate one bit time can be written as:

$$\frac{\text{Osc. Freq.}}{(12) \cdot (\text{baud rate})} = 1 \text{ bit time (in PCA timer ticks)}$$

In this example, the baud rate is 2400 at 16 MHz.

$$\frac{16 \text{ MHz}}{(12) \cdot (2400)} = 556 \text{ counts} = 22\text{C Hex}$$

The high and low byte of this value is placed in the variables FULL_BIT_HIGH and FULL_BIT_LOW, respectively. 115H is the value loaded into HALF_BIT_HIGH and HALF_BIT_LOW.



Listing 1. Variables used by the software serial port. Channel 0

```

;
; Receive Routine
;
RCV_START_BIT_0  BIT    20H.0    ; Indicates start bit
;                               ; has been received
RCV_DONE_0       BIT    20H.1    ; Indicates data byte
;                               ; has been received
RCV_BUF_0        DATA  30H      ; Software Receive
;                               ; "SBUF"
RCV_REG_0        DATA  31H      ; Temporary register
;                               ; for receive bits
RCV_COUNT_0      DATA  32H      ; Counter for receiving
;                               ; bits

; Transmit Routine:
;
TXM_START_BIT_0  BIT    20H.3    ; Indicates start bit
;                               ; has been transmitted
TXM_IN_PROGRESS_0 BIT    20H.4    ; Indicates transmit is
;                               ; in progress
TXM_BUF_0        DATA  34H      ; Software transmit
;                               ; "SBUF"
TXM_REG_0        DATA  35H      ; Temporary register
;                               ; for transmitting bits
TXM_COUNT_0      DATA  36H      ; Counter for transmit-
;                               ; ting bits
DATA_0          DATA  37H      ; Register used for the
;                               ; test program

;
NEG_EDGE         EQU      11H     ; Two modes of operation
S_W_TIMER        EQU      49H     ; for compare/capture
;                               ; modules

;
HALF_BIT_HIGH    EQU      01H     ; Half bit time = 115H
HALF_BIT_LOW     EQU      15H
FULL_BIT_HIGH    EQU      02H     ; Full bit time = 22CH
FULL_BIT_LOW     EQU      2CH     ; 2400 Baud at 16 MHz

```

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Initialization

Listing 2 contains the initialization code for the receive and transmit process. Module 0 of the PCA is used as a receiver and is first set up to detect a negative edge from the start bit. Modules 2 and 3 are used for the additional 2 channels (see the Appendix). Module 3 is used as a separate software timer to transmit bits.

Listing 2. Initialization Routine

```

ORG 0000H
LJMP INITIALIZE
ORG 001BH
LJMP RECEIVE_DONE           ; Timer 1 overflow -
                           ; simulates "RI" interrupt
ORG 0033H
LJMP RECEIVE               ; PCA interrupt
;
INITIALIZE: MOV SP, #5FH    ; Initialize stack pointer
                           ; (specific to test program)
INIT_PCA: MOV CMOD, #00H   ; Increment PCA timer
                           ; @ 1/12 Osc Frequency
                           ; Clear all status flags
                           ; Module 0 in negative-edge
                           ; trigger mode (Pl.3)
                           ; Module 3 as software timer
                           ; mode
MOV CL, #00H
MOV CH, #00H
MOV IE, #0D8H              ; Init all needed interrupts
                           ; EA, EC, ES, ET1
SETB CR                    ; Turn on PCA Counter

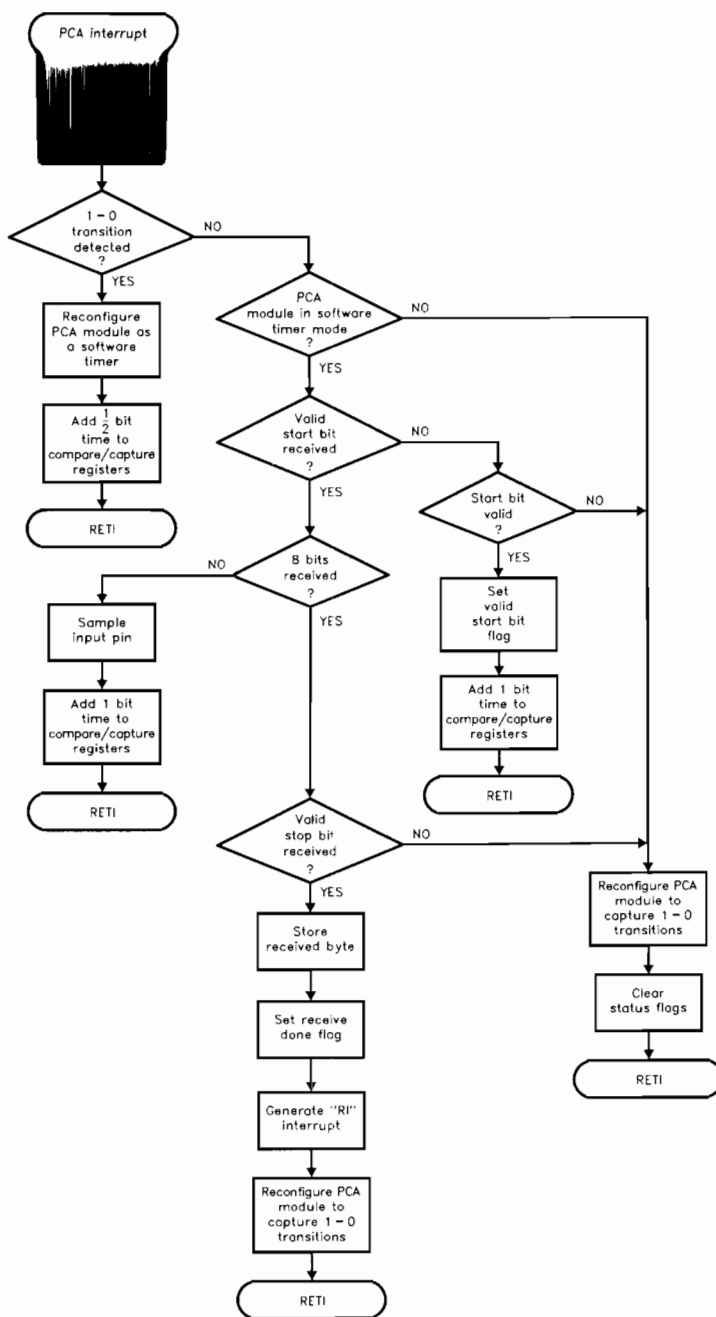
```

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All flags and registers from Listing 1 should be cleared in the initialization process.

Receive Routine

Two operating modes of the PCA are needed to receive bits. The module must first be able to detect the leading edge of a start bit so it is initially set up to capture a 1-to-0 transition (i.e. Negative-Edge Capture mode). The module is then reconfigured as a software timer to cause an interrupt at the center of each bit to deserialize the incoming data. The flowchart for the receive routine is given in Figure 1.



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Figure 1. Flowchart for the Receive Routine

Listing 3.1 shows the code needed to detect a start bit. Notice that the first software timer interrupt will occur one-half bit time after the leading edge of the start bit to check its validity. If it is valid, the RCV_START_BIT is set. The rest of the samples will occur a full bit time later. The RCV_COUNT register is loaded with a value of 9 which indicates the number of bits to be sampled: 8 data bits and 1 stop bit.

Listing 3.1. Receive Interrupt Routine

```

RECEIVE:  PUSH ACC
          PUSH PSW
;
MODULE_0: CLR CCF0           ; Assume reception on
          ; Module 0
          MOV A, CCAPM0       ; Check mode of module. If
          ANL A, #01111111B   ; set up to receive negative
          CJNE A, #NEG_EDGE, RCV_START_0 ; edges, then module
          ; is waiting for a start bit
;
          CLR C               ; Update compare/capture
          MOV A, #HALF_BIT_LOW ; registers for half bit time
          ADD A, CCAP0L        ; to sample start bit
          MOV CCAP0L, A        ; Half bit time = 115H
          MOV A, #HALF_BIT_HIGH
          ADDC A, CCAP0H
          MOV CCAP0H, A
          MOV CCAPM0, #S_W_TIMER ; Reconfigure module 0 as
          POP PSW              ; a software timer to sample
          POP ACC              ; bits
          RETI
;
RCV_START_0: CJNE A, #S_W_TIMER, ERROR_0 ; Check module is
          ; configured as a software
          ; timer, otherwise error.
          JB RCV_START_BIT_0, RCV_BYTE_0 ; Check if start bit
          ; is Received yet.
          JB P1.3, ERROR_0           ; Check that start bit = 0,
          ; otherwise error.
          SETB RCV_START_BIT_0       ; Signify valid start bit
          ; was received
          MOV RCV_COUNT_0, #09H      ; Start counting bits sampled
;
          CLR C                       ; Update compare/capture
          MOV A, #FULL_BIT_LOW        ; registers to sample
          ADD A, CCAP0L                ; incoming bits
          MOV CCAP0L, A                ; Full bit time = 22CH
          MOV A, #FULL_BIT_HIGH
          ADDC A, CCAP0H
          MOV CCAP0H, A
          POP PSW
          POP ACC
          RETI

```

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The next 8 timer interrupts will receive the incoming data bits; the RCV_COUNT register keeps track of how many bits have been sampled. As each bit is sampled, it is shifted through the Carry Flag and saved in RCV_REG. The ninth sample checks the validity of the stop bit. If it is valid, the data byte is moved into RCV_BUF.

The main routine must have a way to know that a byte has been received. With the on-chip UART, the RI (Receive Interrupt) bit is set whenever a byte has been received. For the software serial port, any unimplemented interrupt vector can be used to generate an interrupt when a byte has been received. This routine uses the Timer 1 Overflow interrupt (its selection is arbitrary). A routine to test this interrupt is included in the listing in the Appendix.

Listing 3.2. Receive Interrupt Routine (Continued)

```
RCV_BYTE_0: DJNZ RCV_COUNT_0, RCV_DATA_0 ; On 9th sample,
                                           ; check for valid stop bit
RCV_STOP_0: JNB P1.3, ERROR_0
             MOV RCV_BUF_0, RCV_REG_0 ; Save received byte in
                                           ; receive "SBUF"
             SETB RCV_DONE_0          ; Flag which module received
                                           ; a byte
             SETB TF1                 ; Generate an interrupt so
                                           ; main program knows a byte
                                           ; has been received
                                           ; (Note: selection of TF1 is
                                           ; arbitrary)
             MOV CCAPM0, #NEG_EDGE    ; Reconfigure module 0 for
                                           ; Reception of a start bit
             POP PSW
             POP ACC
             RETI

;
RCV_DATA_0: MOV C, P1.3               ; Sampling data bits
             MOV A, RCV_REG_0         ; Shifts bits thru CY into
             RRC A                    ; ACC
             MOV RCV_REG_0, A         ; Save each reception in
                                           ; temporary register
             CLR C                     ; Update c/c register for
             MOV A, #FULL_BIT_LOW     ; next sample time
             ADD A, CCAP0L
             MOV CCAP0L, A
             MOV A, #FULL_BIT_HIGH
             ADDC A, CCAP0H
             MOV CCAP0H, A
             POP PSW
             POP ACC
             RETI
```

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In addition, an error routine (Listing 3.3) is included for invalid start or stop bits to offer some protection against noise. If an error occurs, the module is re-initialized to look for another start bit.

Listing 3.3 Error Routine for Receive Routine

```
ERROR_0: MOV CCAPM0, #NEG_EDGE ; Reset module to look for
                                ; start bit
             CLR RCV_START_BIT_0 ; Clear flags which might
                                ; have been set
             POP PSW
             POP ACC
             RETI
```

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Transmit Routine

Another PCA module is configured as a software timer to interrupt the CPU every bit time. With each timer interrupt one or more bits can be transmitted through port pins. In the test program three channels were operated simultaneously, but in the listings below, one channel is shown for simplicity. The selection of port pins is user programmable. The flowchart for the transmit routine is given in Figure 2.

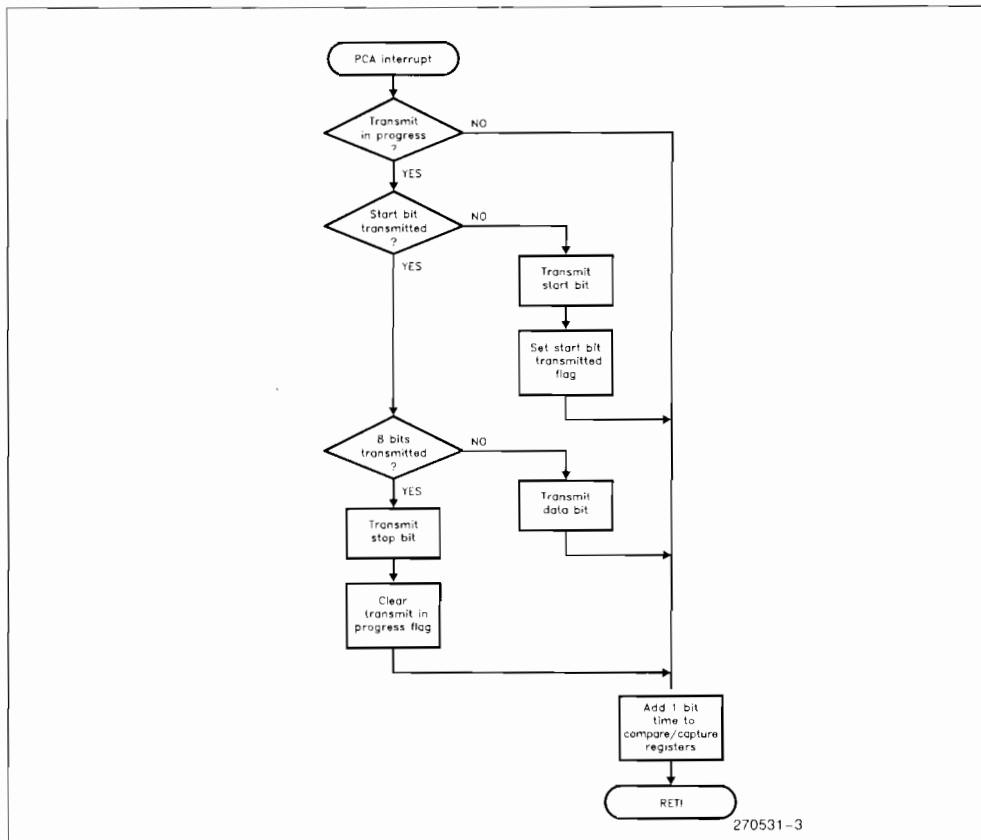


Figure 2. Flowchart for the Transmit Routine

When a byte is ready to be transmitted, the main program moves the data byte into the TXM_BUF register and sets the corresponding TXM_IN_PROGRESS bit. This bit informs the interrupt routine which channel is transmitting. The data byte is then moved in the storage register TXM_REG, and the TXM_COUNT is loaded. This main routine is shown in Listing 4.1.

Listing 4.1 Transmit Set Up Routine. Channel 0.

```

TXM_ON_0: CLR TXM_START_BIT_0    ; Clear status flag from
                                ; previous transmission
          MOV TXM_BUF_0, DATA_0  ; Load "SBUF" with data byte
          MOV TXM_REG_0, TXM_BUF_0
          MOV TXM_COUNT_0, #09    ; 8 data bits + 1 stop bit
          SETB TXM_IN_PROGRESS_0
  
```

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Listing 4.2 shows the transmit interrupt routine. The first time through, the start bit is transmitted. As each successive interrupt outputs a bit, the contents of TXM_REG is shifted right one place into the Carry flag, and the TXM_COUNT is decremented. When TXM_COUNT equals zero, the stop bit is transmitted.

Listing 4.2. Transmit Interrupt Routine

```

TRANSMIT: PUSH ACC
          PUSH PSW
          CLR CCF3                ; Clear s/w timer interrupt
                                   ; for transmitting bits
          JNB TXM_IN_PROGRESS_0, TRANSMIT_1 ; Check which
                                   ; channel is transmitting.
                                   ; "TRANSMIT 1" is listed in
                                   ; the Appendix
;
TRANSMIT_0: JB TXM_START_BIT_0, TXM_BYTE_0 ; If start bit
                                   ; has been sent, continue
                                   ; transmitting bits.
          CLR P3.2                ; Otherwise transmit start
                                   ; bit
          SETB TXM_START_BIT_0    ; Signify start bit sent
          JMP TXM_EXIT
;
TXM_BYTE_0: DJNZ TXM_COUNT_0, TXM_DATA_0 ; If bit count
                                   ; equals 1 thru 9, transmit
                                   ; data bits (8 total)
;
TXM_STOP_0: SETB P3.2            ; When bit count = 0,
                                   ; transmit stop bit
          CLR TXM_IN_PROGRESS_0 ; Indicate transmission is
                                   ; finished and ready for
                                   ; next byte
          JMP TXM_EXIT
;
TXM_DATA_0: MOV A, TXM_REG_0      ; Transmit one bit at a time
          RRC A                  ; through the carry bit
          MOV P3.2, C
          MOV TXM_REG_0, A        ; Save what's not been sent
;
TXM_EXIT: CLR C                  ; Update compare value with
          MOV A, #FULL_BIT_LOW   ; Full bit time = 22CH
          ADD A, CCAP3L
          MOV CCAP3L, A
          MOV A, #FULL_BIT_HIGH
          ADDC A, CCAP3H
          MOV CCAP3H, A
          POP PSW
          POP ACC
          RETI

```

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Conclusion

The software routines in the Appendix can be altered to vary the baud rate and number of channels to fit a particular application. The number of channels which can be implemented is limited by the CPU time required to service the PCA interrupt. At higher baud rates, fewer channels can be run.

The test program verifies the simultaneous operation of three half-duplex channels at 2400 Baud and the on-chip full-duplex channel at 9600 Baud. Thirty-three percent of the CPU time is required to operate all four channels. The test was run for several hours with no apparent malfunctions.

APPENDIX

01/01/80 PAGE 1

MCS-51 MACRO ASSEMBLER SW:PORT
 DOS 3.26 (038-N) MCS-51 MACRO ASSEMBLER, V2.2
 C:\MCS51\BIN\MCS51AS1.EXE
 ASSEMBLER INVOKED BY: C:\MCS51\AS1.EXE SW:PORT.RCV

```

LOC OBJ          TIME SOURCE
1 2 SNOWD51
2 3 SNCSYMBOLS
3 4 SNOLIST
4 5
5 6 ; This program tests the receive routines of a software serial port.
6 7 ; Three half-duplex channels are implemented in software to run at
7 8 ; 2400 baud (16Mhz). The on-chip serial port is also running full-duplex
8 9 ; at 9600 baud. Thirty-three percent of the CPU time is required to run
9 10 ; all four ports simultaneously.
10 11 ; To test the receive routines, "dummy" terminals transmit 00 - FF hex
11 12 ; continually to the PCA. When the first byte is received, it is
12 13 ; compared with 00. If the comparison is valid, the compare value is
13 14 ; incremented and the routine waits to receive the next byte. Error
14 15 ; routines toggle LEDs on ports 1 and 2 if an invalid comparison occurs
15 16 ; or if an invalid start bit or stop bit is received.
16 17
17 18 ORG 00H
18 19 LAMP INITIALIZE
19 20
20 21 ORG 0019H
21 22 LAMP RECEIVE_DONE
22 23
23 24 ORG 0023H
24 25 LAMP SERIAL_PORT
25 26
26 27 ORG 0033H
27 28 LAMP RECEIVE
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MCS-51 MACRO ASSEMBLER SMF0RT

LOC	OBJ	LINE	SOURCE
0030		199	RCV_BUF_0
0040		200	RCV_BUF_1
0050		201	RCV_BUF_2
0031		203	RCV_REG_0
0041		204	RCV_REG_1
0051		205	RCV_REG_2
0032		206	RCV_COUNT_0
0042		207	RCV_COUNT_1
0052		208	RCV_COUNT_2
0033		210	COUNT_0
0043		211	COUNT_1
0053		212	COUNT_2
0011		213	NEG_EDGE
0049		216	S_W_TIMER
0015		217	HALF_BIT_LOW
0031		218	HALF_BIT_HIGH
002C		219	FULL_BIT_LOW
0062		220	FULL_BIT_HIGH
		221	
		222	
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		224	
		225	
		226	
		227	
		228	
0036 75015F		230	INITIALIZE:
		231	INIT_PCA:
0039 750900		232	MOV SP, #5FH
003C 750800		233	MOV CCON, #00H
003F 750A11		234	MOV CCON, #NEG_EDGE
0042 750B14		235	MOV CCON, #NEG_EDGE
0045 750C11		236	MOV CCON, #NEG_EDGE
		237	
0048 75E900		238	MOV CL, #00H
004B 75F900		239	MOV CH, #00H
004E 75A808		240	SETB CH
0051 D2DE		241	
		242	
0053 759850		243	INIT_SP:
0056 75C8FF		244	MOV RCAP2H, #0FFH
0059 75C9CC		245	MOV RCAP2L, #0CCH
005C 75C934		246	MOV I2CON, #34H
		247	
005F C200		248	INIT_FLAGS:
0061 C208		249	CLR RCV_START_BIT_0
0063 C210		250	CLR RCV_START_BIT_1
		251	CLR RCV_START_BIT_2
0065 C201		252	CLR RCV_DONE_0
		253	

30B	; Software receive "SBUF"
40H	
50H	
31H	; Temporary register for
41H	; receiving bits
51H	
32H	; Counter for receiving bits
42H	
52H	
33H	; Used in test program to check
43H	; bytes being received
53H	
11H	; Two modes of operation for the
49H	; Compare/Capture modules
15H	; Half bit time = 115H
07H	
2CH	; Full bit time = 22CH
02H	
	; 2400 Baud @ 16MHz

INITIALIZATION ROUTINE

=====

	; Initialize stack pointer
	; (specific to the test program)
	; Increment PCA clock @ 1/12 Osc Freq
	; Clear all status flags
	; Module 0 in Neg-edge capture mode [P1.3]
	; Module 1 in Neg-edge capture mode [P1.4]
	; Module 2 " " " " [P1.5]
	; Initialize needed interrupt: EA, EC, ES, ET1
	; Turn on PCA counter
	; Serial port in mode 1 (8-Bit UART)
	; Reload values for 9600 Baud @ 16 MHz
	; Timer 2 as a baud-rate generator,
	; turn on timer 2

SWPORT

SOURCE

[illegible]

MAIN TEST ROUTINE - RECEIVE BITS

```

; main program continually checks
; each channel for a received byte.
CNAME A, COUNT 0, ERROR0
CLR RCV ON 1, ERROR1
INC COUNT 0

UNB RCV ON 1, CHECK 2
MOV A, RCV BUF 1
CNAME A, COUNT 1, ERROR1
CLR RCV ON 1, ERROR1
INC COUNT 1

UNB RCV ON 2, CHECK 0
MOV A, RCV BUF 2
CNAME A, COUNT 2, ERROR2

```


LOC	OBJ	LINE	SOURCE
0111 32		364	RETI
0112 8494B		365	RCV_START_0:
015 20001A		366	CJNE A, #S_TIMER, ERROR_0
018 209345		367	JB RCV_START_BIT_0, RCV_BYTE_0
011B 0200		368	JB P1.3, ERROR_0
011D 753209		369	SETB RCV_START_BIT_0
0120 C3		370	MOV RCV_COUNT_0, #09H
0121 742C		371	CLR C
0122 8494B		372	MOV A, #FULL_BIT_LOW
0123 753A		373	MOV A, C
0124 742C		374	MOV A, C
0125 753A		375	MOV A, #FULL_BIT_HIGH
0126 753A		376	ADDC A, C
0127 753A		377	MOV A, C
0128 753A		378	MOV A, C
0129 753A		379	MOV A, C
012A 753A		380	MOV A, C
012B 753A		381	MOV A, C
012C 753A		382	MOV A, C
012D 753A		383	MOV A, C
012E 753A		384	MOV A, C
012F 753A		385	MOV A, C
0130 753A		386	MOV A, C
0131 32		387	RETI
0132 D53212		388	RCV_BYTE_0:
0135 109328		389	RCV_STOP_0:
0138 851130		390	JNB P1.3, ERROR_0
013B 0201		391	MOV RCV_BUF_0, RCV_REG_0
013D 028F		392	SETB RCV_DONE_0
013F 750A11		393	SETB T1
0142 0000		394	MOV CCAPM0, #NEG_EDGE
0144 0060		395	POP PSW
0146 32		396	POP ACC
0147 A293		397	RETI
0149 2531		398	RCV_DATA_0:
014B 13		399	MOV C, P1.3
014C F531		400	MOV A, RCV_REG_0
014E C3		401	RRC A
014F 742C		402	MOV RCV_REG_0, A
0151 256A		403	CLR C
0153 753A		404	MOV A, #FULL_BIT_LOW
0155 7402		405	ADD A, C
0157 753A		406	MOV A, C
0158 0200		407	ADD A, C
0159 0200		408	MOV A, C
015A 0200		409	ADD A, C
015B 0200		410	MOV A, C
015C 0200		411	ADD A, C
015D 0200		412	MOV A, C
015F 32		413	POP PSW
0160 C2B5		414	POP ACC
		415	RETI
		416	ERROR_0:
		417	CLR P3.5

MCS-51 MACRO ASSEMBLER SUPPORT

LOC	OBJ	LINE	SOURCE
0162	75B11	418	
0163	C209	419	MOV CCAPM0, INEG_EDGE
0164	D0D0	420	CLR RCV_START_BIT_0
0165	D0E0	421	POP PSM
0166	D0E0	422	POP ACC
0167	D0E0	423	RET
0168	32	424	
0169	D0E0	425	
0170	D0E0	426	
0171	D0E0	427	
0172	B4115	428	CHANNEL 1
0173	C3	429	-----
0174	7415	430	
0175	7415	431	
0176	7415	432	
0177	7415	433	
0178	7415	434	
0179	7415	435	
0180	7415	436	
0181	7415	437	
0182	7415	438	
0183	7415	439	
0184	7415	440	
0185	7415	441	
0186	7415	442	
0187	7415	443	
0188	7415	444	
0189	32	445	
0190	7415	446	
0191	7415	447	
0192	7415	448	
0193	D208	449	
0194	7415	450	
0195	754209	451	
0196	C3	452	
0197	742C	453	
0198	25E8	454	
0199	742C	455	
0200	742C	456	
0201	742C	457	
0202	742C	458	
0203	742C	459	
0204	742C	460	
0205	742C	461	
0206	742C	462	
0207	742C	463	
0208	742C	464	
0209	742C	465	
0210	742C	466	
0211	742C	467	
0212	742C	468	
0213	742C	469	
0214	742C	470	
0215	742C	471	
0216	742C	472	

MCS-51 MACRO ASSEMBLER SNMPORT

LOC	OBJ	LINE	SOURCE
0210	C3	58	CLR C
0211	742C	59	MOV A, #FULL_BIT_LOW
0212	7551	60	ADD A, CCAP2H, A
0213	75EC	61	MOV CCAP2H, A
0214	7602	62	MOV A, #FULL_BIT_HIGH
0215	76FC	63	ADD A, CCAP2H, A
0216	7702	64	MOV CCAP2H, A
0217	77FC	65	POP PSM
0218	7802	66	POP ACC
0219	78FC	67	RETI
0220	7902	68	DJNZ RCV_COUNT_2, RCV_DATA_2
0221	79FC	69	RCV_BYTE_2:
0222	D5512	70	MOV RCV_BUF_2, RCV_REG_2
0223	309528	71	SETB RCV_DONE_2
0224	85150	72	SETB TF1
0225	D211	73	MOV CCAP2H, #NEG_EDGE
0226	D28F	74	POP PSM
0227	73DC11	75	POP ACC
0228	7402	76	RETI
0229	74FC	77	MOV C, P1.5
0230	D8E0	78	MOV A, RCV_REG_2
0231	32	79	MOV RCV_REG_2, A
0232	32	80	CLR C
0233	C3	81	MOV A, #FULL_BIT_LOW
0234	742C	82	ADD A, CCAP2H, A
0235	7551	83	MOV CCAP2H, A
0236	75EC	84	MOV A, #FULL_BIT_HIGH
0237	7602	85	ADD A, CCAP2H, A
0238	76FC	86	MOV CCAP2H, A
0239	7702	87	POP PSM
0240	77FC	88	POP ACC
0241	D0D0	89	RETI
0242	D0D0	90	ERROR_2:
0243	32	91	CLR P3.7
0244	32	92	MOV CCAP2H, #NEG_EDGE
0245	C2B7	93	CLR RCV_START_BIT_2
0246	75DC11	94	POP PSM
0247	C210	95	POP ACC
0248	D0D0	96	RETI
0249	D0D0	97	;
0250	32	98	;
0251	32	99	;
0252	32	100	;
0253	32	101	;
0254	32	102	;
0255	32	103	;
0256	32	104	;
0257	32	105	;
0258	32	106	;
0259	32	107	;
0260	32	108	;
0261	32	109	;
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0263	32	111	;
0264	32	112	;
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0270	32	118	;
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0280	32	128	;
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MCS-51 MACRO ASSEMBLER

UNOS 3.20 (038-N) MCS-51 MACRO ASSEMBLER, V2.2

OBJECT MODULE PLACED IN SWPRT.OBJ
ASSEMBLER INVOKED BY: C:\AEDIT\ASMS1.EXE SWPRT.TR

LOC	OR	LINE	SOURCE
1	1	1	1
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100	100	100	100

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ORG 00H

VARIABLES USED BY THE SOFTWARE SERIAL PORT

MCS-51 MACRO ASSEMBLER SUPPORT

LOC	OBJ	LINE	SOURCE	DATA	5/H
199			DATA 2		
200	0057		5_W_TIMER	EQ	49H
201	0049		FULL_BIT_LOW	EQ	2CH
202	002C		FULL_BIT_HIGH	EQ	02H
203	0002				
204			INITIALIZATION		
205			*****		
206					
207					
208					
209					
210	0036 75815F		INIT_TMX:	MOV SP, #5FH	
211				MOV CMOD, #00H	
212	0039 759900			MOV CCN, #00H	
213	003C 75D800			MOV CH, #00H	
214	003E 75E800			MOV CCAPM3, #5_W_TIMER	
215	003F 75E800			MOV IE, #008H	
216	0045 750D49			MOV SCN, #50H	
217				MOV RCAP2H, #0FFH	
218	0048 75A808			MOV RCAP2L, #00CH	
219				MOV TZCON, #134H	
220	004B 759050		INIT_SP:	CLR TMX_START_BIT 0	
221	004E 7588FF			CLR TMX_START_BIT 1	
222	0051 75ACCC			CLR TMX_IN_PROGRESS 0	
223	0054 75C834			CLR TMX_IN_PROGRESS 1	
224				CLR TMX_IN_PROGRESS 2	
225	0057 C203		INIT_FLAGS:	MOV TMX_BUF 0, #00H	
226	0059 C208			MOV TMX_BUF 1, #00H	
227	005B C213			MOV TMX_BUF 2, #00H	
228				MOV TMX_REC 0, #00H	
229	005D C204			MOV TMX_REC 1, #00H	
230	005F C20C			MOV TMX_REC 2, #00H	
231	0061 C214			MOV TMX_COUNT 0, #00H	
232				MOV TMX_COUNT 1, #00H	
233	0063 753400			MOV DATA 0, #01FH	
234	0066 754400			MOV DATA 1, #0FFH	
235	0069 755400			MOV DATA 2, #0FFH	
236					
237	006C 753500				
238	006F 754500				
239	0072 755500				
240					
241	0075 753600				
242	0078 754600				
243	007B 755600				
244					
245	007E 7537FF				
246	0081 7547FF				
247	0084 7557FF				
248					
249	0087 75E02C				
250	008A 75E02C				
251	008D 75E02C				
252					
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01/01/80

SWF00T      MCS-51 MACRO ASSEMBLER

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MCS-51 MACRO ASSEMBLER SUPPORT

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LOC      OBJ      SOURCE
LINE
309      TXM_BYTE_0:  DJNZ TXM_COUNT_0, TXM_DATA_0
310
311      TXM_STOP_0:   SETB P3.2
312                      CLR TXM_IN_PROGRESS_0
313                      JNB TXM_START_BIT_1, TXM_BYTE_1
314                      JMP TXM_TRANSMIT_1
315
316      TXM_DATA_0:   MOV A, TXM_REG_0
317                      RRC A, 1
318                      MOV TXM_REG_0, A
319                      JMP TXM_TRANSMIT_1
320
321      TXM_BYTE_1:  DJNZ TXM_COUNT_1, TXM_DATA_1
322
323      TXM_STOP_1:   SETB P3.3
324                      CLR TXM_IN_PROGRESS_1
325                      JMP TXM_TRANSMIT_2
326
327      TXM_DATA_1:   MOV A, TXM_REG_1
328                      RRC A, 1
329                      MOV TXM_REG_1, A
330                      JMP TXM_TRANSMIT_2
331
332      TXM_BYTE_2:  DJNZ TXM_COUNT_2, TXM_DATA_2
333
334      TXM_STOP_2:   SETB P3.4
335                      CLR TXM_IN_PROGRESS_2
336                      JMP TXM_TRANSMIT_2
337
338      TXM_DATA_2:   MOV A, TXM_REG_2
339                      RRC A, 1
340                      MOV TXM_REG_2, A
341                      JMP TXM_TRANSMIT_2
342
343      TXM_BYTE_3:  DJNZ TXM_COUNT_3, TXM_DATA_3
344
345      TXM_STOP_3:   SETB P3.5
346                      CLR TXM_IN_PROGRESS_3
347                      JMP TXM_TRANSMIT_2
348
349      TXM_DATA_3:   MOV A, TXM_REG_3
350                      RRC A, 1
351                      MOV TXM_REG_3, A
352                      JMP TXM_TRANSMIT_2
353
354      TXM_BYTE_4:  DJNZ TXM_COUNT_4, TXM_DATA_4
355
356      TXM_STOP_4:   SETB P3.6
357                      CLR TXM_IN_PROGRESS_4
358                      JMP TXM_TRANSMIT_2
359
360      TXM_DATA_4:   MOV A, TXM_REG_4
361                      RRC A, 1
362                      MOV TXM_REG_4, A
363                      JMP TXM_TRANSMIT_2
364
365      TXM_BYTE_5:  DJNZ TXM_COUNT_5, TXM_DATA_5
366
367      TXM_STOP_5:   SETB P3.7
368                      CLR TXM_IN_PROGRESS_5
369                      JMP TXM_TRANSMIT_2
370
371      TXM_DATA_5:   MOV A, TXM_REG_5
372                      RRC A, 1
373                      MOV TXM_REG_5, A
374                      JMP TXM_TRANSMIT_2
375
376      TXM_BYTE_6:  DJNZ TXM_COUNT_6, TXM_DATA_6
377
378      TXM_STOP_6:   SETB P3.7
379                      CLR TXM_IN_PROGRESS_6
380                      JMP TXM_TRANSMIT_2
381
382      TXM_DATA_6:   MOV A, TXM_REG_6
383                      RRC A, 1
384                      MOV TXM_REG_6, A
385                      JMP TXM_TRANSMIT_2
386
387      TXM_BYTE_7:  DJNZ TXM_COUNT_7, TXM_DATA_7
388
389      TXM_STOP_7:   SETB P3.7
390                      CLR TXM_IN_PROGRESS_7
391                      JMP TXM_TRANSMIT_2
392
393      TXM_DATA_7:   MOV A, TXM_REG_7
394                      RRC A, 1
395                      MOV TXM_REG_7, A
396                      JMP TXM_TRANSMIT_2
397
398      TXM_BYTE_8:  DJNZ TXM_COUNT_8, TXM_DATA_8
399
400      TXM_STOP_8:   SETB P3.7
401                      CLR TXM_IN_PROGRESS_8
402                      JMP TXM_TRANSMIT_2
403
404      TXM_DATA_8:   MOV A, TXM_REG_8
405                      RRC A, 1
406                      MOV TXM_REG_8, A
407                      JMP TXM_TRANSMIT_2
408
409      TXM_BYTE_9:  DJNZ TXM_COUNT_9, TXM_DATA_9
410
411      TXM_STOP_9:   SETB P3.7
412                      CLR TXM_IN_PROGRESS_9
413                      JMP TXM_TRANSMIT_2
414
415      TXM_DATA_9:   MOV A, TXM_REG_9
416                      RRC A, 1
417                      MOV TXM_REG_9, A
418                      JMP TXM_TRANSMIT_2
419
420      TXM_BYTE_10: DJNZ TXM_COUNT_10, TXM_DATA_10
421
422      TXM_STOP_10:  SETB P3.7
423                      CLR TXM_IN_PROGRESS_10
424                      JMP TXM_TRANSMIT_2
425
426      TXM_DATA_10:  MOV A, TXM_REG_10
427                      RRC A, 1
428                      MOV TXM_REG_10, A
429                      JMP TXM_TRANSMIT_2
430
431      TXM_BYTE_11: DJNZ TXM_COUNT_11, TXM_DATA_11
432
433      TXM_STOP_11:  SETB P3.7
434                      CLR TXM_IN_PROGRESS_11
435                      JMP TXM_TRANSMIT_2
436
437      TXM_DATA_11:  MOV A, TXM_REG_11
438                      RRC A, 1
439                      MOV TXM_REG_11, A
440                      JMP TXM_TRANSMIT_2
441
442      TXM_BYTE_12: DJNZ TXM_COUNT_12, TXM_DATA_12
443
444      TXM_STOP_12:  SETB P3.7
445                      CLR TXM_IN_PROGRESS_12
446                      JMP TXM_TRANSMIT_2
447
448      TXM_DATA_12:  MOV A, TXM_REG_12
449                      RRC A, 1
450                      MOV TXM_REG_12, A
451                      JMP TXM_TRANSMIT_2
452
453      TXM_BYTE_13: DJNZ TXM_COUNT_13, TXM_DATA_13
454
455      TXM_STOP_13:  SETB P3.7
456                      CLR TXM_IN_PROGRESS_13
457                      JMP TXM_TRANSMIT_2
458
459      TXM_DATA_13:  MOV A, TXM_REG_13
460                      RRC A, 1
461                      MOV TXM_REG_13, A
462                      JMP TXM_TRANSMIT_2
463
464      TXM_BYTE_14: DJNZ TXM_COUNT_14, TXM_DATA_14
465
466      TXM_STOP_14:  SETB P3.7
467                      CLR TXM_IN_PROGRESS_14
468                      JMP TXM_TRANSMIT_2
469
470      TXM_DATA_14:  MOV A, TXM_REG_14
471                      RRC A, 1
472                      MOV TXM_REG_14, A
473                      JMP TXM_TRANSMIT_2
474
475      TXM_BYTE_15: DJNZ TXM_COUNT_15, TXM_DATA_15
476
477      TXM_STOP_15:  SETB P3.7
478                      CLR TXM_IN_PROGRESS_15
479                      JMP TXM_TRANSMIT_2
480
481      TXM_DATA_15:  MOV A, TXM_REG_15
482                      RRC A, 1
483                      MOV TXM_REG_15, A
484                      JMP TXM_TRANSMIT_2
485
486      TXM_BYTE_16: DJNZ TXM_COUNT_16, TXM_DATA_16
487
488      TXM_STOP_16:  SETB P3.7
489                      CLR TXM_IN_PROGRESS_16
490                      JMP TXM_TRANSMIT_2
491
492      TXM_DATA_16:  MOV A, TXM_REG_16
493                      RRC A, 1
494                      MOV TXM_REG_16, A
495                      JMP TXM_TRANSMIT_2
496
497      TXM_BYTE_17: DJNZ TXM_COUNT_17, TXM_DATA_17
498
499      TXM_STOP_17:  SETB P3.7
500                      CLR TXM_IN_PROGRESS_17
501                      JMP TXM_TRANSMIT_2
502
503      TXM_DATA_17:  MOV A, TXM_REG_17
504                      RRC A, 1
505                      MOV TXM_REG_17, A
506                      JMP TXM_TRANSMIT_2
507
508      TXM_BYTE_18: DJNZ TXM_COUNT_18, TXM_DATA_18
509
510      TXM_STOP_18:  SETB P3.7
511                      CLR TXM_IN_PROGRESS_18
512                      JMP TXM_TRANSMIT_2
513
514      TXM_DATA_18:  MOV A, TXM_REG_18
515                      RRC A, 1
516                      MOV TXM_REG_18, A
517                      JMP TXM_TRANSMIT_2
518
519      TXM_BYTE_19: DJNZ TXM_COUNT_19, TXM_DATA_19
520
521      TXM_STOP_19:  SETB P3.7
522                      CLR TXM_IN_PROGRESS_19
523                      JMP TXM_TRANSMIT_2
524
525      TXM_DATA_19:  MOV A, TXM_REG_19
526                      RRC A, 1
527                      MOV TXM_REG_19, A
528                      JMP TXM_TRANSMIT_2
529
530      TXM_BYTE_20: DJNZ TXM_COUNT_20, TXM_DATA_20
531
532      TXM_STOP_20:  SETB P3.7
533                      CLR TXM_IN_PROGRESS_20
534                      JMP TXM_TRANSMIT_2
535
536      TXM_DATA_20:  MOV A, TXM_REG_20
537                      RRC A, 1
538                      MOV TXM_REG_20, A
539                      JMP TXM_TRANSMIT_2
540
541      TXM_BYTE_21: DJNZ TXM_COUNT_21, TXM_DATA_21
542
543      TXM_STOP_21:  SETB P3.7
544                      CLR TXM_IN_PROGRESS_21
545                      JMP TXM_TRANSMIT_2
546
547      TXM_DATA_21:  MOV A, TXM_REG_21
548                      RRC A, 1
549                      MOV TXM_REG_21, A
550                      JMP TXM_TRANSMIT_2
551
552      TXM_BYTE_22: DJNZ TXM_COUNT_22, TXM_DATA_22
553
554      TXM_STOP_22:  SETB P3.7
555                      CLR TXM_IN_PROGRESS_22
556                      JMP TXM_TRANSMIT_2
557
558      TXM_DATA_22:  MOV A, TXM_REG_22
559                      RRC A, 1
560                      MOV TXM_REG_22, A
561                      JMP TXM_TRANSMIT_2
562
563      TXM_BYTE_23: DJNZ TXM_COUNT_23, TXM_DATA_23
564
565      TXM_STOP_23:  SETB P3.7
566                      CLR TXM_IN_PROGRESS_23
567                      JMP TXM_TRANSMIT_2
568
569      TXM_DATA_23:  MOV A, TXM_REG_23
570                      RRC A, 1
571                      MOV TXM_REG_23, A
572                      JMP TXM_TRANSMIT_2
573
574      TXM_BYTE_24: DJNZ TXM_COUNT_24, TXM_DATA_24
575
576      TXM_STOP_24:  SETB P3.7
577                      CLR TXM_IN_PROGRESS_24
578                      JMP TXM_TRANSMIT_2
579
580      TXM_DATA_24:  MOV A, TXM_REG_24
581                      RRC A, 1
582                      MOV TXM_REG_24, A
583                      JMP TXM_TRANSMIT_2
584
585      TXM_BYTE_25: DJNZ TXM_COUNT_25, TXM_DATA_25
586
587      TXM_STOP_25:  SETB P3.7
588                      CLR TXM_IN_PROGRESS_25
589                      JMP TXM_TRANSMIT_2
590
591      TXM_DATA_25:  MOV A, TXM_REG_25
592                      RRC A, 1
593                      MOV TXM_REG_25, A
594                      JMP TXM_TRANSMIT_2
595
596      TXM_BYTE_26: DJNZ TXM_COUNT_26, TXM_DATA_26
597
598      TXM_STOP_26:  SETB P3.7
599                      CLR TXM_IN_PROGRESS_26
600                      JMP TXM_TRANSMIT_2
601
602      TXM_DATA_26:  MOV A, TXM_REG_26
603                      RRC A, 1
604                      MOV TXM_REG_26, A
605                      JMP TXM_TRANSMIT_2
606
607      TXM_BYTE_27: DJNZ TXM_COUNT_27, TXM_DATA_27
608
609      TXM_STOP_27:  SETB P3.7
610                      CLR TXM_IN_PROGRESS_27
611                      JMP TXM_TRANSMIT_2
612
613      TXM_DATA_27:  MOV A, TXM_REG_27
614                      RRC A, 1
615                      MOV TXM_REG_27, A
616                      JMP TXM_TRANSMIT_2
617
618      TXM_BYTE_28: DJNZ TXM_COUNT_28, TXM_DATA_28
619
620      TXM_STOP_28:  SETB P3.7
621                      CLR TXM_IN_PROGRESS_28
622                      JMP TXM_TRANSMIT_2
623
624      TXM_DATA_28:  MOV A, TXM_REG_28
625                      RRC A, 1
626                      MOV TXM_REG_28, A
627                      JMP TXM_TRANSMIT_2
628
629      TXM_BYTE_29: DJNZ TXM_COUNT_2
```

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MCS-51 MACRO ASSEMBLER SWPORT

```

LOC OBJ      LINE      SOURCE
TXM EXIT:
364          CLR C      ; FULL BIT LOW
365          ADD A, CCAP3H
366          MOV C, A
367          MOV A, CCAP3H
368          MOV A, FULL BIT HIGH
369          ADDC A, CCAP3H
370          MOV CCAP3H, A
371          POP PSW
372          POP ACC
373          RETI
374          ;
375          ;
376          ;
377          ;
378          ;
379          ; When a byte is received on the full-duplex serial port, it is then
380          ; transmitted back to a "dummy" terminal. This terminal checks that
381          ; the byte it transmitted to the PCA is the same value it receives back.
382          ;
383          ;
384          SERIAL PORT:
385          PUSH ACC
386          UNB RI, TXM
387          MOV A, SBUF
388          MOV SBUF, A
389          POP PSW, A
390          POP PSW
391          POP ACC
392          RETI
393          ;
394          TXM:
395          POP PSW
396          POP ACC
397          RETI
398          ;
399          ;
400          END

```

REGISTER BANK(S) USED: 0
 ASSEMBLY COMPLETE, NO ERRORS FOUND

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